NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, 83 or 98
Dk MUST MEET THE FOLLOWING CRITERIA 4.0< Dk < 4.5

Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - TRACES WITH 0.020" WIDTH SHALL BE 50 OHM SINGLE ENDED
5a. THE TRACES INDICATED IN DETAIL B WITH AN ARROW ARE CRITICAL DIMENSION AND SHALL MEET 20 +/- 0.1 MILS WIDE.

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.005

7. PLATING FINISH - BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
.05080-.232 MICRON (2-8 MICROINCH) OF GOLD OVER
2.540-6.350 MICRON (100-250 MICROINCH) OF NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.
FILL ALL 6 MIL VIAS WITH NON-CONDUCTIVE EPOXY.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.
MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS,
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. ADD TEARDROPS TO ALL SIGNAL LAYERS.

15. SOLDER SAMPLES TO BE PROVIDED.

16. BASIC GRID INCREMENT AT 1:1 IS .0001.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
- MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (e6)

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM.

21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURING REQUIREMENT.

22. FOR COSMETIC ACCEPTANCE CRITERIA ALSO REFER TO DOC-31008. DOC-31008 HAS PRECEDENCE OVER IPC.

23. COMPONENTS J4 AND C19 SHARE PINS.

24. OVERALL PCB DIELECTRIC THICKNESS ARE TARGETED (A & C) 10 MILS+/- 10% AND (B) 38 MILS+/- 10%
AS SHOWN IN DETAIL 'A'.
ADJUSTMENT OF SUBSTRATE B IS ALLOWED TO MEET OVERALL HEIGHT REQUIREMENT

25. THIS LINE ON TOP LAYER (X=-69, Y=1766) IS INTENTED TO BE CONNECTED TO RF_ANTENNA NET AND GND

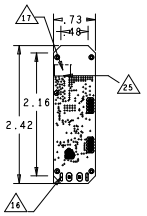
26. INTENTIONAL SHORTS:

SH1	PTB0_KW38	PTB0_K22
SH2	PTB1_KW37	PTB1_K22
SH3	PTB2_KW37	PTB2_K22
SH4	RST_TGTMCU_B	RST_TCTMCU_B_K22F
SH5	PTB3_KW37	PTC6_K22
SH6	PTB18_KW37	PTC7_K22
SH7	K22_SS	PTC19
SH8	K22_SCK	PTC16
SH9	K22_SIN	PTC17
SH10	SPI_SOUT	N24135995
SH11	SPI_SIN	N24135997
SH13	P3V3_KW37	P3V3_K22F
SH14	P3V3_KW37	VDCDC_IN
SH15	P3V3_LED	P3V3_KW22F
SH16	PTC17	SI
SH17	PTC16	SCK
SH18	PTC19	CS
SH19	PTC18	SO
SH20	PTC18	K22_SOUT
SH21	UART_RTS	UART1_CTS_K22F
SH22	UART_CTS	UART1_RTS_K22F
SH23	UART_TXD	UART1_RX_K22F
SH24	UART_RXD	UART1_TX_K22F
ANT1	RF_ANT	GND

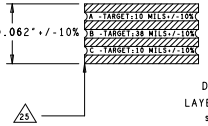
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	X2	ORIGINAL RELEASE	02-27-19	A.Q
	A	PROTOTYPE RELEASE	03-05-19	A.Q
	A1	BOM UPDATE/SILKSCREEN UPDATE	10-30-19	A.Q

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
◉	6.0	+0.0/-6.0	PLATED	39
+	8.0	+0.0/-8.0	PLATED	75
+	8.0	+2.0/-2.0	PLATED	148
⊗	26.0	+2.0/-2.0	PLATED	20
⊕	40.0	+3.0/-3.0	PLATED	1
⊗	39.0	+2.0/-2.0	NON-PLATED	2
⊗	80.0	+2.0/-2.0	NON-PLATED	4
▯	133.0x43.0	+3.0/-3.0	PLATED	2



PRIMARY SIDE VIEW



LAYER 1	COMPONENT SIDE	1	oz.
LAYER 2	GROUND PLANE	1	oz.
LAYER 3	POWER PLANE	1	oz.
LAYER 4	SOLDER SIDE	1	oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE 50 OHMS

___ PUBI (PUBLIC INFORMATION)
X NIUO (NXP INTERNAL USE ONLY)
___ NCP (NXP CONFIDENTIAL PROPRIETARY)

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±.5°
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS, REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

APPROVALS	DATE
DRAWN: A QUIROZ	03-05-19
CHECKED: M BAUDRY	03-05-19
DESIGN ENGINEER: A QUIROZ.	03-05-19

PART NO. 170-43114

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
USB-KW38

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-43114	FAB-43114	A1

SCALE: DO NOT SCALE DRAWING SHEET OF